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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/777,897	02/07/01	TANIGUCHI N	100353-00039

MMC2/0906
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EXAMINER	
NGUYEN,L	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/06/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/777,897	TANIGUCHI, NOBUTAKA	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 February 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

The drawings are objected to because:

Figure 5, item 22; change "DITECTION" to -- DETECTION --.

Correction is required.

Specification Objections

The specification is objected to because:

Page 11, line 25, change "12" to -- 4 --.

Correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Lu (U.S. Patent No. 6,100,735).

With respect to claims 1-2, and 5, Figures 1 and 7B-C of Lu show a delay time adjusting circuit and a respective method for adjusting a delay time of an input [ICLK]

signal so that a phase of the input signal and a phase of an output signal [DCLK] match each other; the delay time adjusting circuit comprises a) detecting means [14] for detecting a phase difference between the phase of the input signal and the phase of the output signal, and b) delaying means [12,20] for delaying the phase of the output signal until the phase difference becomes N periods, where N is an integer other than zero.

With respect to claim 3, Figures 1 and 7B-C of Lu show a respective adjusting method for adjusting a delay time of an input [ICLK] first periodic signal so that a phase of the input first periodic signal and a phase of an output second periodic signal match each other; the method comprises a step of adjusting [18] the delay time so that when a phase of a predetermined rising edge of the output second periodic signal is behind a phase of a predetermined rising edge of the input first periodic signal, the predetermined rising edge of the output second periodic signal matches a rising edge of the input first periodic signal, and a phase of the rising edge is behind and nearest to the phase of the predetermined rising edge of the output second periodic signal.

With respect to claims 4 and 6, Figures 1 and 7B-C of Lu show a delay adjusting circuit for adjusting a delay time of an input [ICLK] first periodic signal so that a phase of the input first periodic signal and a phase of an output [DCLK] second periodic period match each other; the delay adjusting circuit comprises: a) judging means [14] for judging whether a phase of a predetermined rising edge of the output second periodic signal is behind a phase of a predetermined rising edge of the input first periodic signal, and b) delaying means [12, 20] for adjusting the delay time so that when the phase of the predetermined rising edge of the output second periodic signal is judged to be

behind the phase of the predetermined rising edge of the input first periodic signal by the judging means, the predetermined rising edge of the output second periodic signal matches a rising edge of the input first periodic signal, and a phase of the rising edge is behind and nearest to the phase of the predetermined rising edge of the output second periodic signal.

With respect to claim 7, Figures 1 and 7B-C of Lu show a delay time adjusting circuit for adjusting a delay time of an input [ICLK] first periodic signal so that a phase of the input first periodic signal and a phase of an output [DCLK] second periodic signal match each other; the delay time adjusting circuit comprises a) delaying means [12,20] for delaying the input first periodic signal so as to generate the output second periodic signal, b) a phase-detecting means [14] for detecting whether a phase of a predetermined rising edge of the output second periodic signal is behind a phase of a first rising edge of the input first periodic signal, and c) adjusting means [18] for controlling the delaying means so that when the phase of the predetermined rising edge is judged to be behind the phase of the first rising edge by the detecting means, the delaying means delays the phase of the output second periodic signal until the phase of the determined rising edge and a phase of a second rising edge of the input first periodic signal match each other, and the second rising edge is one period behind the first rising edge.

With respect to claim 8, Figures 1 and 7B-C of Lu show that the adjusting means [18] controls the delaying means [12, 20] so that, after the phase of the predetermined rising edge and the phase of the second rising edge match each other, the phase of the

predetermined rising edge and the phase of the second rising edge match each other all the time within a tolerable range.

Citation of Relevant Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Kaneko (U.S. Patent No. 6,249,188) discloses an error-suppressing phase comparator.

Prior art Takai (U.S. Patent No. 6,069,508) discloses a clock generating circuit having high resolution of delay time between external clock signal and internal clock signal.

Prior art Kawasaki et al. (U.S. Patent No. 6,066,969) discloses a semiconductor device with DLL circuit avoiding excessive power consumption.

Prior art Takemae et al. (U.S. Patent No. 6,028,816) discloses a system configured of synchronous semiconductor device for adjusting timing of each input and semiconductor device used therefore.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (703) 305-0414. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:30 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703) 308-4876. The fax phone

numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Linh M. Nguyen

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800